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**UNITED STATES DISTRICT COURT**  
**NORTHERN DISTRICT OF CALIFORNIA**

12 **MEDIA TEK INC.,**

13 **Plaintiff,**

14 **vs.**

15 **FREESCALE SEMICONDUCTOR, INC.,**

16 **Defendant.**  
17

Case No.: 11-cv-5341 YGR

**ORDER GRANTING IN PART AND DENYING IN  
PART FREESCALE'S MOTION FOR SUMMARY  
JUDGMENT AS TO NON-INFRINGEMENT OF  
THE '845 PATENT AND '331 PATENT**

18 Defendant Freescale Semiconductor, Inc. ("Freescale") filed its Motion for Summary  
19 Judgment on November 6, 2013, moving for summary judgment on several grounds. (Dkt. No. 303.)  
20 The Court previously ruled on Freescale's motion for summary judgment on certain grounds: (1)  
21 denying the motion on its affirmative defense of non-infringement due to the extraterritorial nature of  
22 certain alleged infringing activities and related cross-claim for declaratory relief on the same grounds  
23 (Dkt. No. 444); and (2) denying summary judgment on MediaTek's request for injunctive relief. The  
24 Court now turns to the remaining issues, namely Freescale's motion for summary judgment on  
25 MediaTek's claims of infringement of U.S. Patent Nos. 6,738,845 ("845 Patent") and 6,889,331  
26 ("331 Patent").

27 Having carefully considered the papers submitted, the admissible evidence, and the pleadings  
28 in this action, and for the reasons set forth below, the Court hereby orders that the Motion for

Summary Judgment of Non-Infringement is **GRANTED IN PART AND DENIED IN PART**. The motion for a determination of non-infringement of Claim 35 of the '331 Patent by the accused **i.MX31, i.MX35, and i.MX50 chips**, is **GRANTED**. All other grounds for summary judgment are **DENIED**.

**I. APPLICABLE LAW**

Summary judgment is appropriate where there are no genuine disputes as to material facts and the moving party is entitled to judgment as a matter of law. Fed. R. Civ. P. 56(a). A fact is material if it might affect the outcome of the suit, and a dispute is genuine only if there is a sufficient evidentiary basis for a reasonable jury to return a verdict for the nonmoving party. *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986); *In re Barboza*, 545 F.3d 702, 707 (9th Cir. 2008).

The court must view the facts in the light most favorable to party opposing summary judgment, giving that party the benefit of all reasonable inferences from those facts. *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986); *Anderson*, 477 U.S. at 255. The opposing party must show that genuine dispute exists “by citing to particular parts of materials in the record.” Fed. R. Civ. P. 56(c)(1)(A). An opposing party’s “bald assertions or a mere scintilla of evidence in his favor are both insufficient to withstand summary judgment.” *F.T.C. v. Stefanchik*, 559 F.3d 924, 929 (9th Cir. 2009).

Here, the legal issue is patent infringement. A person directly infringes a patent by making, using, offering to sell, selling, or importing into the United States any patented invention, without authority, during the term of the patent. 35 U.S.C. § 271. Patent infringement analysis is a two-step process. *Read Corp. v. Portec, Inc.*, 970 F.2d 816, 821-22 (Fed. Cir. 1992). In the first step, the court construes the patent claim terms asserted to be infringed. *Id.* at 821; *Senmed, Inc. v. Richard-Allan Medical Indus., Inc.*, 888 F.2d 815, 818 (Fed. Cir. 1989). In the second step, the court compares the construed patent claims to the accused method or product. *Fonar Corp. v. Johnson & Johnson*, 821 F.2d 627, 631-32 (Fed. Cir. 1987). If the claims cover the accused product or process in a literal way, there is literal infringement. A patent claim “reads on” a product or process if that product or process contains each limitation of the claim. *Jurgens v. McKasy*, 927 F.2d 1552, 1560

(Fed. Cir. 1991). Literal infringement is a question of fact. *SSIH Equip. S.A. v. United States Int'l Trade Comm'n*, 718 F.2d 365, 376 (Fed. Cir. 1983).

“Where the parties do not dispute any relevant facts regarding an accused product,” “but disagree over possible claim interpretations, the question of literal infringement collapses into claim construction and is amenable to summary judgment.” *General Mills, Inc. v. Hunt-Wesson, Inc.*, 103 F.3d 978, 983 (Fed. Cir. 1997). For a defendant seeking summary judgment of non-infringement, “nothing more is required than the filing of a ... motion stating that the patentee had no evidence of infringement and pointing to the specific ways in which accused [products] did not meet the claim limitations.” *Exigent Tech., Inc. v. Atrana Solutions, Inc.*, 442 F.3d 1301, 1309 (Fed. Cir. 2006).

The Court first addresses Freescale’s motion for non-infringement of the ‘845 Patent: (1) Claims 1, 2, and 5 with respect to Freescale’s i.MX6 family of chips; and (2) Claims 21, 22 and 25 with respect to i.MX51 and i.MX53 chips, specifically the “same priority level” and “greater portion of the available bandwidth” limitations. The Court then turns to Freescale’s motion for non-infringement as to the ‘331 Patent: (1) Claim 35 with respect to the i.MX31, i.MX35, and i.MX50 chips practicing the “power supply” limitation; and (2) Claim 11 with respect to the i.MX31, i.MX35, i.MX50, and i.MX6 chips practicing the “plurality of registers” and “clock frequency requirement” limitations.

## **II. NON-INFRINGEMENT OF THE ‘845 PATENT**

The object of the ‘845 Patent is to provide an architecture for arrangement of components in a small multiple data processor system, such as a mobile phone. (Ewerdt Decl., Exh. 1, Dkt. No. 303-9, “‘845 Patent”, col. 1:15-17.) Components making processing or data demands within the system are called “masters” and components responding or providing the data are called “slaves.” The “set of signal paths connecting the functional units of the circuit” are called “busses.” (‘845 Patent, col. 2:24-25.) Also relevant here are bus arbitration units, i.e. units which “arbitrate” various requests for access by the references components. In Freescale’s motion for summary judgment on the ‘845 Patent, the two sets of claims at issue specify two aspects of the bus architecture described in the patent.

**A. Claims 1, 2, and 5: Alleged Infringement by Freescale's i.MX6 Family of Chips**

The first claimed aspect as to which Freescale seeks a determination of non-infringement stems from a dispute over the scope of the bus arbitration units described in independent Claim 1 and incorporated into dependent Claims 2 and 5. ('845 Patent, col. 9:65-10:21.) Claim 1 of the '845 patent identifies a specific arbitration limitation which Freescale claims its products do not perform. Thus it recites: "a first arbitration unit associated with the first slave subsystem ... configured and arranged to arbitrate among at least the first data processing subsystem, the second data processing subsystem, and the DMA [direct memory access] subsystem for access to the first slave subsystem." ('845 Patent, col. 9:65-10:9, quoted portion italicized in note.)<sup>1</sup>

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<sup>1</sup> Claim 1 reads, in part:

1. A system, comprising:
  - a first data processing subsystem comprising a first processor coupled to a first bus as a first bus master;
  - a second data processing subsystem comprising a second processor coupled to a second bus as a second bus master;
  - a direct memory access (DMA) subsystem comprising a DMA controller coupled to a third bus as a third bus master;
  - a first slave subsystem comprising a memory unit coupled to a fourth bus;
  - a second slave subsystem comprising a fifth bus;
  - a first arbitration unit associated with the first slave subsystem, having each of the first, second, third and fourth busses coupled thereto, *configured and arranged to arbitrate among at least the first data processing subsystem, the second data processing subsystem, and the DMA subsystem for access to the first slave subsystem*, and to couple the fourth bus to any selected one of at least the first, second, and third busses so as to enable a selected one of at least the first data processing subsystem, the second data processing subsystem, and the DMA subsystem to access the first slave subsystem; and
  - a second arbitration unit associated with the second slave subsystem, having each of the first, second, third and fifth busses coupled thereto, configured and arranged to arbitrate among at least the first data processing subsystem, the second data processing subsystem, and the DMA subsystem for access to the second slave subsystem, and to couple the fifth bus to any selected one of at least the first, second, and third busses so as to enable a selected one of at least the first data processing subsystem, the second data processing subsystem, and the DMA subsystem to access the second slave subsystem ... .

Figure 3 of the '845 Patent illustrates the configuration of components as described in Claim

1. Arbitration units (314, 315, and 316, outlined in orange) are each associated with different slave

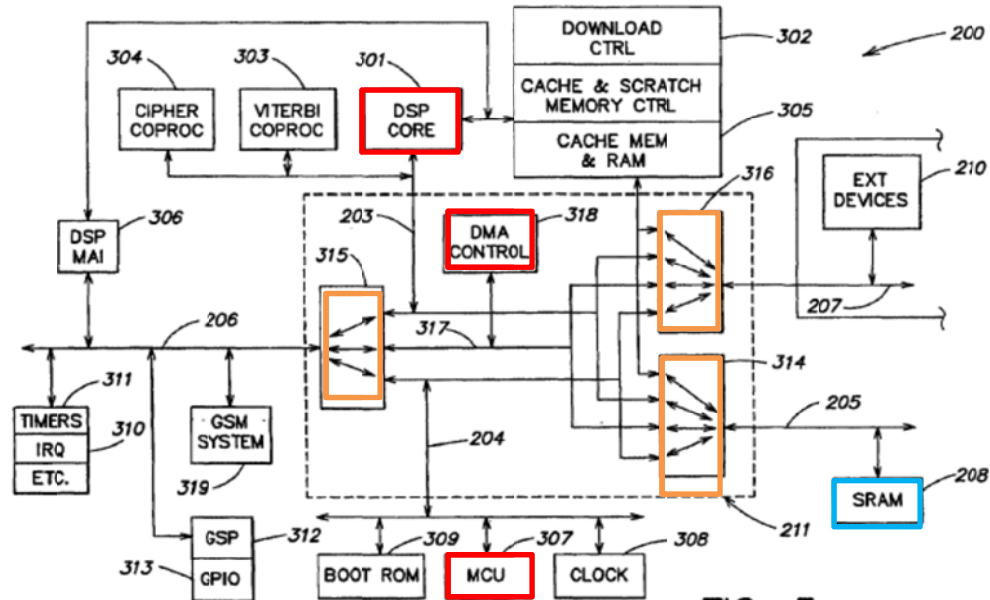


FIG. 3

components. For example, the SRAM at 208 (outlined in blue) is associated with unit 314.

Arbitration units 314 and 316 must arbitrate among the three required masters —two data processors (shown in Figure 3 as the DSP Core, 301, and the MCU, 307, outlined in red) and the DMA controller (318, outlined in red) – for access to an associated slave subsystem component, like the SRAM. At issue in this motion is the question of whether the accused chips have a component that arbitrates “among” a first data processing subsystem, a second data processing subsystem, and a DMA subsystem for access to a (first) slave subsystem, as stated in Claim 1.

Freescall argues that its i.MX6 family of chips (i.MX6DQ, i.MX6SDL, and i.MX6SL) do not infringe asserted Claims 1, 2, and 5 of the '845 patent because they do not arbitrate “among at least the first data processing subsystem, the second data processing subsystem, and the DMA subsystem for access to the first slave subsystem,” as required. The accused arbitration unit of the i.MX6 chips never arbitrates between two separate data processing subsystems and a DMA subsystem. Instead,

1 requests from the two data processing subsystems are arbitrated by another arbiter before they reach  
2 the alleged “first arbitration unit,” here the MX6FAST3.

3 MediaTek counters that it has submitted evidence establishing that the i.MX6 chips practice  
4 the “first arbitration unit” limitation of Claim 1 in the infringement report of their expert, Dr. Krste  
5 Asanovic. Asanovic opines that the “DQ” and “SDL” product lines include a NIC-301 arbiter  
6 component within the MX6FAST3 which fits the “first arbitration unit” limitation. In his expert  
7 report, Asanovic posits as follows: The NIC-301 of MX6FAST3 arbitrates for access to a memory  
8 unit called the OCRAM, the “first slave subsystem.” The MX6FAST3 arbitrates among an ARM  
9 processor (“first data processing subsystem”), an Image Processing Unit (IPU) (“second data  
10 processing subsystem”), and a Smart DMA (SDMA) (“DMA subsystem”) for access to the OCRAM.  
11 Requests from the ARM, IPU, and SDMA must pass through the FAST3 arbitration unit in order to  
12 access the OCRAM. Asanovic testified that the MX6FAST3 stores requests from both the ARM and  
13 the IPU and arbitrates between the requests for access to the OCRAM. (Asanovic Decl. Exh. 2, at  
14 461:16-462:9.) As to the i.MX6SL product, MediaTek argues that it contains another NIC-301  
15 arbiter that meets the “first arbitration unit” limitation of ’845 patent claim 1. Thus, Asanovic’s  
16 expert report sets forth facts supporting his opinion that the i.MX6SL’s NIC-301 arbiter arbitrates  
17 among the ARM (“first data processing subsystem”), a second data processing subsystem, and a  
18 SDMA subsystem for access to the memory unit. (Asanovic Dec. ¶ 7, Asanovic Report Exh D-2, at  
19 44-46.)

20 The Court finds that determination of this issue requires claim construction as to the meaning  
21 of the term “among” as it is used in the phrase “configured and arranged to arbitrate among ... the  
22 first data processing subsystem, the second data processing subsystem, and the DMA subsystem for  
23 access to the first slave subsystem....” The crux of the disagreement here turns on whether the  
24 arbitration unit can be said to arbitrate “among” the three master components if requests pass through  
25 a separate arbiter before accessing the OCRAM. MediaTek’s position looks backward from the  
26 OCRAM and sees that the FAST3 arbiter decides “among” requests that may come from any of the  
27 three components. In other words, the FAST3 arbiter is the “last stop” for requests coming from any  
28 of these components before they can be forwarded to the slave subsystem they all seek to access.

1 Freescale's view is forward-looking, contending that the FAST3 never arbitrates as between three  
2 different requests from the three components at the same time, but instead another arbiter decides  
3 requests between two components and sends them on to FAST3 for arbitration after that. In other  
4 words, in Freescale's view, the arbiter is not deciding "among" the requests unless requests from all  
5 components are before it at the same time. Thus, Freescale's expert agreed that the FAST3 is what  
6 allows access to the OGRAM by any one of the ARM, the IPU, and the SDMA, albeit with the  
7 caveat that another arbitration has occurred prior to the one in the FAST3. (Vahid Tr. 279:7-12;  
8 280:12-16.)<sup>2</sup>

9 Freescale's use of the "among" narrows its application without providing any support for  
10 such a construction. "A patentee may claim an invention broadly and expect enforcement of the full  
11 scope of that language absent a clear disavowal" of that language either in the specifications or the  
12 prosecution history. *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1357 (Fed. Cir. 2004).  
13 Freescale, the party with the burden to establish that it is entitled to summary judgment, has failed to  
14 submit any evidence on this point. Further, MediaTek has offered evidence in opposition that creates  
15 disputed issues of material fact based on its contended construction. That is, MediaTek's expert has  
16 opined that the elements of Claim 1 are practiced by the accused products, consistent with  
17 MediaTek's understanding of the Claim 1 language.

18 That Freescale's expert disagrees with this opinion is unsurprising, given the competing  
19 views regarding the scope of the term "among." The Court reserves on the issue of construction to  
20 the extent ultimately an issue. *Jack Guttman, Inc. v. Kopykake Enterprises, Inc.*, 302 F.3d 1352,  
21 1361 (Fed. Cir. 2002) ("courts may engage in a rolling claim construction, in which the court revisits

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22  
23 <sup>2</sup> A problematic aspect of Freescale's motion is that, while conceding that the MX6FAST3 is  
24 an arbiter, it does not explain what it is that the FAST3 is arbitrating if *not* requests from the three  
25 components. The diagrams offered in Freescale's motion do not show what components send  
26 requests to FAST3, and indeed seem to leave out important details considered by Asanovic in his  
27 analysis of the i.MX6 chips with respect to Claim 1. (Cf. Asanovic Report Exh. D-2 at 42 ¶3,  
28 describing the connection of the third bus to FAST3.) The diagrams offered in the brief appear to be  
oversimplifications that neglect to depict the expert opinions accurately.

and alters its interpretation of the claim terms as its understanding of the technology evolves”) (citing *Sofamor Danek Group, Inc. v. DePuy–Motech, Inc.*, 74 F.3d 1216, 1221 (Fed.Cir.1996)). However, it is a dispute of facts that cannot be decided on summary judgment.<sup>3</sup> Summary judgment on this issue is **DENIED**. This order does not preclude the Court from ordering a construction later in the proceedings.

**B. Claims 21, 22 and 25: Alleged Infringement of i.MX51 and i.MX53 Chips**

The feature at issue in independent Claim 21, and dependent Claims 22 and 25, of the ‘845 Patent is the use of a bus arbitration module, or BAM. Here, the patent claims a system for two data processing subsystems to access the same slave subsystem.<sup>4</sup> The BAM must enable “first and

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<sup>3</sup> The question of whether Asanovic properly can offer his opinion that the NIC-301 arbiters here buffer requests from two masters is really a red herring. Asanovic conceded that he had not specifically identified the internal buffers discussion as part of the report on his infringement opinion with respect to Claims 1, 2, and 5 of the ‘845 Patent. (Ewerdt Decl. Exh. 2 (Asanovic Depo., Dkt. 348-10) 471:11-23.) However, the buffer issue only came up because he was asked if the FAST3 arbiter could arbitrate between *simultaneous* requests. As Asanovic stated in his deposition, he did not believe that the limitations of Claim 1 required simultaneous requests, but buffering could explain how requests from three different components might be arbitrated at the same time. (Asanovic Depo. 470:6-473:18.)

MediaTek’s objection to the new evidence offered in reply regarding the buffering capabilities of the NIC-301 arbiters is well taken. The Court agrees that this evidence was improperly submitted, given that Asanovic testified to his buffering opinion in connection with his deposition held October 17 and 18, 2013, well before Freescale filed its summary judgment motion on November 6, 2013. *Contratto v. Ethicon, Inc.*, 227 F.R.D. 304, 308, n.5 (N.D. Cal, 2005); *In re High-Tech Employee Antitrust Litig.*, 11-cv-02509-LHK, 2013 WL 5770992, at \*6, n.4 (N.D. Cal. Oct. 24, 2013). The Court notes that Freescale did not object to or move to strike Asanovic’s evidence concerning buffering in the NIC-301 arbiters in connection with Claims 1, 2, and 5 of the ‘845 Patent. Such a motion at this late juncture would be barred as untimely.

<sup>4</sup> Claim 21 reads:  
A system, comprising:  
a first data processing subsystem comprising a first processor coupled to a first bus as a first bus master;  
a second data processing subsystem comprising a second processor coupled to a second bus as a second bus master;  
a first slave subsystem comprising a memory unit coupled to a third bus;  
a second slave subsystem comprising a fourth bus; and  
*cont’d...*

second data processing subsystems to access different ones of the first and second slave subsystems at the same time” and must be “further configured and arranged” such that, when “all requests for access” to one of the slave subsystems “are of the same priority level,” one of the “data processing subsystems is guaranteed to have access to a greater portion of the available bandwidth” than the other. (*See italicized portion of fn.4.*)

Freescall argues that the accused i.MX51 and i.MX53 chips do not infringe because they lack the claimed “BAM” arbitration technique required by Claims 21, 22, and 25. More precisely, Freescall argues its accused products are not configured to employ the sole arbitration scheme that MediaTek argues infringes.

### *1. Same Priority Level*

First, the claimed arbitration scheme requires “period[s] when all requests for access to ... slave subsystems are of the same priority level....” (’845 Patent, col. 12:65-13:27.) In its infringement allegations with respect to Claims 21, 22, and 25, MediaTek has accused the ARM and the IPU in Freescall’s i.MX51 and i.MX53 chips of satisfying the first data processor and second data processor limitations, respectively. (Ewerdt Decl. Exh. 15, Rule 3-1 Disclosure, Exh. A-1, at 26-31; Ewerdt Decl. Exh. 3, ’845 Infr. Rpt, Exh. D1, at 2-12.) The ARM and IPU are alleged to send requests to an arbitration unit, ARB1, for simultaneous access to a second slave subsystem. (’845 Infr. Rpt, Exh. D1, at 15-34.)

(...cont’d)

a bus arbitration module (BAM), having the first, second, third, and fourth busses coupled thereto, configured and arranged to couple each of the third and fourth busses to any selected one of at least the first and second busses so that each of first and second slave subsystems can be independently accessed by either of the first and second data processing subsystems, ***thereby enabling the first and second data processing subsystems to access different ones of the first and second slave subsystems at the same time, the BAM being further configured and arranged to employ an arbitration scheme for access*** to at least a first one of the first and second slave subsystems in which, during any period when all requests for access to the first one of the first and second slave subsystems are ***of the same priority level, a first one*** of the first and second data processing subsystems is ***guaranteed to have access to a greater portion of the available bandwidth*** of the first one of the first and second slave subsystems than is a second one of the first and second data processing subsystems.

Freescall seeks summary judgment on this infringement allegation on the grounds that there is no evidence that the arbitration block of the i.MX51 and i.MX53 chips arbitrates between data processing subsystems with the same priority; rather they only arbitrate those with different priorities. According to Freescall, these accused master processors have different, fixed priorities when approaching the arbitrator (ARB1) for access to the slave subsystem. (*See* Freescall's Statement of Undisputed Material Facts ("SUMF"), Dkt. No. 303-7, and evidence cited therein, Facts 25, 28, 31.) Thus, Freescall argues that ARB1 never arbitrates between requests of the same priority from the ARM and the IPU, so that the same priority requirements of Claims 21, 22, and 25 are not satisfied.

MediaTek opposes, arguing that the ARM and IPU in the accused products have a "dynamic priority," not just the fixed priority Freescall describes. MediaTek contends that the evidence shows a dynamic priority mechanism which allows the ARM and the IPU to make requests at the same priority level to the ARB1 arbiter. (MediaTek's Response to SUMF, Dkt. No. 325-8, Facts 28, 31; Chen Decl., Exh. C ("i.MX53 Reference Manual") at FSL-00016536; *id.* Exh. D ("i.MX51 Reference Manual") at FSL-00011007.) MediaTek uses Freescall's reference manuals to confirm: (1) that masters can have a range of possible priorities, with some priorities overlapping, *i.e.* the same; and (2) that the chips' arbitration units will allocate bandwidth between two masters' requests (requests "A" and "B") that are at the same priority level. (*See* Chen Decl. Exh. C, i.MX53 Reference Manual, at FSL-00016536 and FSL-00016541; Exh. D., i.MX51 Reference Manual, at

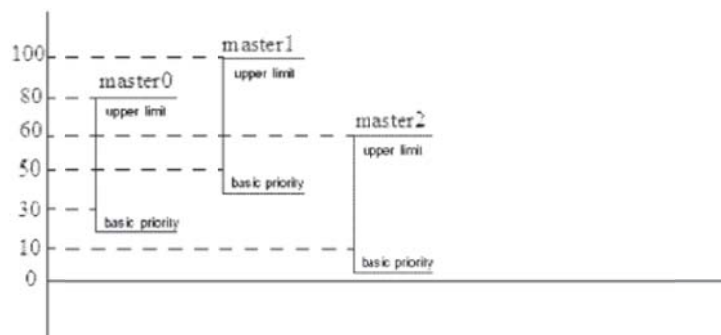


Figure 49-3. Master's Dynamic Priority Scheme

FSL-00011008, Figure 49-3, and FSL-00011012.) The reference manuals include a section titled:

1 “49.2.9 Arbitration Scheme when Masters have Same Priority (Bus Division),” describing an  
2 “arbitration mechanism when the priority of two or more master requests are the same value.”  
3 (i.MX53 Reference Manual at FSL-00016539; i.MX51 Reference Manual, at FSL-00011010.)

4 MediaTek also puts forward evidence that Freescale’s own witnesses testified to the dynamic  
5 priority mechanism allowing these two masters to make requests at the same priority level.  
6 Freescale’s expert conceded in his deposition that it is possible for the ARM and the IPU to make the  
7 requests at the same priority level. (Dkt. No. 325-33 (Vahid Tr.); 506:1-8, 507:8-13, 508:7-16 and  
8 Dkt. 348-8 (Vahid Tr.) at 252:6-16) And Freescale’s Rule 30(b)(6) witness, Allen Wagner, testified  
9 that the accused products include a mechanism for arbitrating requests when two masters have the  
10 same priority. (Chen Dec. Exh. E, Wagner Tr., at 196:10-15.)<sup>5</sup>

11 If the accused products are capable of operating in a way that meets the claim limitations,  
12 even if that is not the usual or default mode of operation, there is infringement. *See Fantasy Sports*  
13 *Properties, Inc. v. Sportsline.com, Inc.*, 287 F.3d 1108, 1118 (Fed. Cir. 2002) (holding infringement  
14 exists when accused software “include[s] the ‘means for scoring ... bonus points’ regardless of  
15 whether that means is activated or utilized in any way”); *Intel Corp. v. U.S. Int’l Trade Comm’n*, 946  
16 F.2d 821, 832 (Fed. Cir. 1991) (holding that, where accused EPROM chips were “capable of  
17 performing page mode addressing,” even though “the EPROMs were never sold to operate in page  
18 mode” and “[n]o customer was ever told how to convert the chip to page mode operation – or even  
19 that such conversion was possible,” “actual page mode operation in the accused device is not  
20 required” for infringement).

21 MediaTek’s evidence is sufficient to create a triable issue of fact as to whether the masters in  
22 the accused products, the ARM and the IPU, are capable of transmitting requests for the same slave  
23 at the same priority level. The evidence reasonably supports an inference that the identified masters  
24

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25 <sup>5</sup> Freescale argues on reply that MediaTek’s reliance on Figure 49-3 from the i.MX51/53  
26 reference manuals is unwarranted since the figure only shows dynamic/variable priority ranges for  
27 three masters— master0, master1, and master2 – and the ARM only connects as master3. However,  
28 Freescale has not submitted evidence to support its argument and it is thus rejected.

1 submit requests at the same priority level for access to the same slave subsystem. Consequently, the  
2 motion is **DENIED**.

3 **2. “Greater Portion of the Available Bandwidth”**

4 Freescale next contends that the accused chips do not meet the limitations of Claim 21 which  
5 guarantee a “greater portion of the available bandwidth” to one subsystem over another when the  
6 subsystems’ requests for access are of the same priority.<sup>6</sup> Freescale’s reading of this language is that  
7 the word “portion” requires that the two data processing subsystems share bandwidth between them  
8 such that each has some amount greater than 0%. In the accused chips, none (0%) of the available  
9 bandwidth of a slave subsystem is assigned to a second data processing subsystem.

10 MediaTek’s response is two-fold: (1) 100% can be a “portion,” and (2) even if a “portion”  
11 has to be something less than 100% and more than 0%, the chips here can be configured and  
12 arranged to use a 75/25 arbitration scheme. (See i.MX53 Reference Manual at FSL-00016541;  
13 i.MX51 Reference Manual at FSL-00011012.) Claim 21 is a “system” claim, not a “method” claim,  
14 and it recites that the bus arbitration module need only be “configured and arranged to employ” the  
15 recited arbitration scheme. MediaTek contends that its evidence shows the ARB1 bus arbitration  
16 module in Freescale’s i.MX51 and i.MX53 products is configured and arranged to employ a 75% /  
17 25% bandwidth allocation scheme.

18 Leaving aside the question of whether 100% can be a “portion,” the fact that the accused  
19 chips can operate with a 75/25 allocation is sufficient to preclude summary judgment. While

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20  
21 <sup>6</sup> Claim 21 reads, in pertinent part,  
22 the BAM being further configured and arranged to employ an arbitration scheme  
23 for access to at least a first one of the first and second slave subsystems in which,  
24 during any period when all requests for access to the first one of the first and  
25 second slave subsystems are of the same priority level, a first one of the first and  
26 second data processing subsystems is *guaranteed to have access to a greater  
portion of the available bandwidth* of the first one of the first and second slave  
subsystems than is a second one of the first and second data processing  
subsystems.

27 (‘845 Patent, col. 13:17-27, emphasis supplied.)  
28

1 Freescale argues 100/0 share scheme is the default, that users are warned against changing the  
2 settings, and that a user must undertake work to change the system to a 75/25 scheme, none of these  
3 arguments change the fact that the chips can be configured to operate in this way. That the products  
4 are able to perform in a manner consistent with Freescale's reading of the claim language creates a  
5 triable issue on infringement by those products. *See Fantasy Sports, supra*, 287 F.3d at 1118; *Intel*  
6 *Corp., supra*, 946 F.2d at 832. Summary judgment is thus properly **DENIED**.

### 7 **III. NON-INFRINGEMENT OF THE '331 PATENT**

8 The '331 Patent concerns a method and an apparatus for reducing power consumption in  
9 processors in devices such as computers and cellular phones. (Ewerdt Decl. Exh. 8, '331 Patent,  
10 1:11-26.) The method and apparatus relate to dynamically controlling the voltage level supplied to a  
11 processor based on its processing state and/or computational demands by determining a clock  
12 frequency requirement and a corresponding voltage requirement. ('331 Patent, col. 1:10-17.) The  
13 '331 Patent includes claims and describes embodiments for: a method; a processor; a "controller" (or  
14 "dynamic power controller"); and a device. The Claims at issue here are the "processor" claim,  
15 independent Claim 11, and the "device" claim, independent Claim 35.

16 Figure 4 of the '331 Patent illustrates one embodiment of the patent, a processor having dynamic  
17 power control capabilities. ('331 Patent, col. 1:40-43.)<sup>7</sup> In Figure 4, the dynamic power control  
18 processor is contained within 20" (outlined in orange), with the dynamic power controller, 100 (in  
19 red), and the clock control component, 110 (in blue), contained therein. ('331 Patent, col. 7:55-64.)  
20 "In FIG. 4, processor 20' is supplied power by off-chip power management 40" outlined in yellow.  
21 (*Id.*, 7:64-66.)

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26  
27 <sup>7</sup> The '331 Patent does not include any figure that is described as being an illustration of an  
28 embodiment of the "device" as stated in Claim 35.

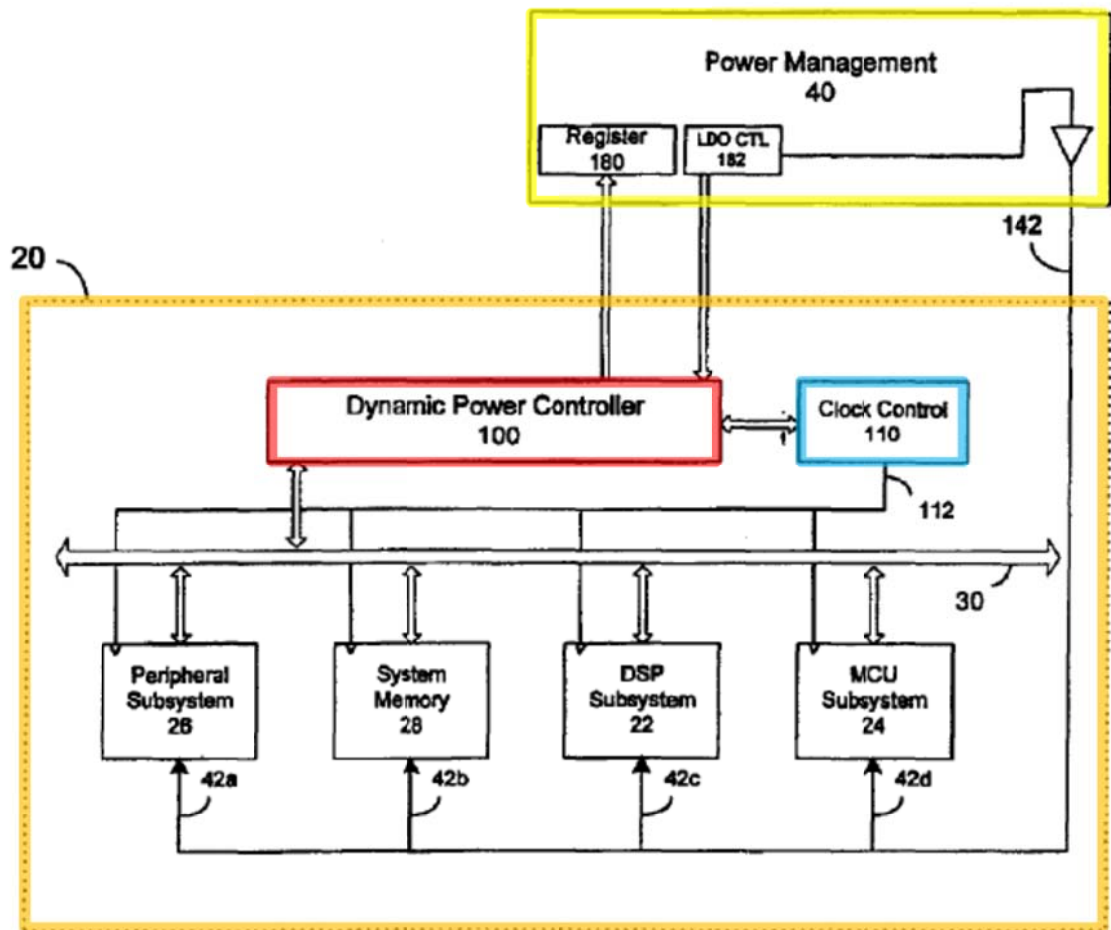


FIGURE 4, '331 PATENT

The '331 Patent describes the power management system as one wherein the dynamic power control block contains the power management components and carries out the power management operations described in the patent. (*Id.*, 8:8-22.) The power management operations of the dynamic power control block are designed to adjust the frequency, or speed, of the clock and the level of voltage supplied to the processor subsystem blocks. (*Id.*, Col. 8:8-22.)

**A. Claim 35: i.MX31, i.MX35, and i.MX50 Chips Alleged Infringement Based Upon Practicing the "Power Supply" Limitation**

Freescle seeks summary judgment of non-infringement as to its accused i.MX31, i.MX35, and i.MX50 chips based upon the argument that the chips lack the "power supply" required by Claim

35 of the '331 patent. (Ewerdt Decl. Exh. 16, MediaTek's Amended Disclosure of Asserted Claims and Infringement Contentions (6/10/2013), Exh. B-1, at 11-12 [hereinafter Rule 3-1 Disclosure, Exh. B-1]; Ewerdt Decl. Exh. 10, '331 Infr. Rpt., Exh. C-1, at 40; Ewerdt Decl. Exh. 11, '331 Infr. Rpt., Exh. C-2, at 31-32.). The claim at issue here, Claim 35 of the '331 Patent, recites a device comprising "a power supply adapted to provide a variable level voltage." ('331 Patent, 18:5.)<sup>8</sup>

Freescall argues that the plain language of Claim 35 requires that the accused chips must include *on the chip itself* a "power supply adapted to provide a variable level voltage" in order to be a "device" that meets all of that claim's limitations. Freescall contends that the accused chips are sold without a PMIC and can be operated "without being attached to an external PMIC." On the latter point, Freescall's expert stated, in his Rebuttal Report, that the accused chips "only require an external *power source* ... [which may be] a variable-voltage PMIC, a single-voltage PMIC or a simple hard-wiring to a battery." (Vahid Rebuttal Report ¶ 343 [emphasis supplied].) Further, MediaTek's expert report implicitly confirms that the source of power for the accused chips is not located *on* the accused chips, but instead is used "*with*" the chips. ('331 Infr. Rpt., Exh. C-1 at 40 [accused i.MX31 and i.MX35 chips "*used with* a Power Management IC (PMIC) that provides a variable level voltage ...."]; Exh. C-2 at 31-32 [same for i.MX50 chip].) Consequently, Freescall contends that the claim limitation is not met.

Freescall's motion starts from the premise that its chips cannot be found to infringe if the "power supply" element is not on the chip itself, but never explains why that is so. First, the language of Claim 35 does not require that anything on the chip itself be the source of the necessary

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<sup>8</sup> Claim 35 reads:

A device comprising:

at least one processor having a plurality of components operating with a plurality of clock signals;

*a power supply adapted to provide a variable level voltage* to the at least one processor; a clock controller adapted to control a frequency of the plurality of clock signals; and a dynamic power controller, connected to the power supply and the clock controller, adapted to monitor the at least one processor to determine a clock frequency requirement of the at least one processor and to determine a voltage requirement based on the clock frequency requirement, and configured to transition the power supply and the clock controller to a power state defined by the clock frequency requirement and the voltage requirement.

1 voltage. Claim 35 does not require that a power source reside on the chip but instead requires that  
 2 there be a power “supply adapted to provide a variable level voltage.” Claim 35 describes a device  
 3 “comprising” several elements, including this “power supply.” Further, the specification of the ‘331  
 4 Patent describes the processor as being “supplied power by off-chip power management” as depicted  
 5 in Fig. 4. (‘331 Patent, col. 7:64-66.) It describes that power management as being capable of  
 6 *residing off-chip*, as in the illustration of Fig. 4, or “*alternatively, located on the same semiconductor*  
 7 *chip as the processor.*” (‘331 Patent, col. 7:65-8:1.) The “Power management 40 [in Fig. 4] may be  
 8 ***any component capable of providing a source*** of power, typically, by providing a voltage level that  
 9 may be specified by the component receiving power.” (*Id.*, col. 8:2-5, emphasis supplied.) Claim 35  
 10 is describing a ***device***. Hence, at least one embodiment in the specification contemplates an off-chip  
 11 power source that must be connected to the chip to power it.

12 In opposition, MediaTek argues that Freescale has misunderstood its infringement theory,  
 13 which does not rely on the external PMIC to meet the “power supply” limitation, but instead  
 14 contends that the limitation is met by “power pins” on the chip that connect to the external power  
 15 source and thereby “supply” power to the chip. Hence, MediaTek contends, the accused chips have  
 16 “power pin[s] that are adapted to provide a variable level voltage from a Power Management IC  
 17 (“PMIC”) to an internal processor.” (MediaTek’s Opposition, Dkt. No. 325-6, at 12:25-26.) In  
 18 support of this argument, MediaTek argues that its expert, Narad, offered this theory in both his  
 19 report and his deposition. Freescale objects that MediaTek is attempting to avoid summary judgment  
 20 by arguing this new power pins theory, which is not found in its Rule 3-1 Disclosure or in Narad’s  
 21 opening expert report.

22 As an initial matter, the Court must look to the claim language to determine its plain  
 23 meaning. Here, the claim states that the “device” of Claim 35 “comprises” several elements,  
 24 including the “power supply” element. “‘Comprising’ is a term of art used in claim language which  
 25 means that the named elements are essential, but other elements may be added and still form a  
 26 construct within the scope of the claim.” *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed.  
 27 Cir. 1997). Thus, because the device of Claim 35 must comprise the “power supply” element, the  
 28 “power supply” must be part of the accused chip itself. MediaTek does not argue otherwise.

1 The Court next looks to the evidence submitted. Contrary to MediaTek's argument in  
 2 opposition, Narad's infringement report does not state the theory that power pins meet the "power  
 3 supply" limitation. To the contrary, his report states the accused products meet the "power supply"  
 4 limitation because they are each:  
 5 used with a Power Management IC (PMIC) that provides a variable level voltage,  
 6 and there is no substantial use of the [accused chips] without such a PMIC. In  
 7 addition, Freescale sells PMIC chips for use with the [accused chips]  
 8 (Dkt. No. 303-26 (Narad '331 Infr. Rpt. Exh. C-1) at 38-39 (emphasis added); Dkt. No. 303-27 (Exh.  
 9 C-2) at 32 (emphasis added).) Mr. Narad's claim charts do not mention "power pins" or state an  
 10 opinion that they meet the "power supply" limitation. MediaTek's infringement contentions are  
 11 likewise silent as to a contention that "power pins" constitute the "power supply." (Dkt. No. 306-16,  
 12 MediaTek Amended Infringement Contentions, Exh. B-1, at 12-13; *id.* Exh. B-2 at 11.) The closest  
 13 the infringement contentions come to even mentioning a "power pins" aspect of the accused chips is  
 14 a citation to i.MX50 Reference Manual at Chapter 58. That reference manual mentions "extal and  
 15 xtal pins." (Dkt. 332-9, i.MX50 Multimedia Applications Processor Reference Manual at  
 16 FSL00009016 et seq., Exh. 2 to Franklin Decl.) However, the reference in the infringement  
 17 contentions is not repeated or discussed in Narad's report. The infringement contentions, plainly, are  
 18 not evidence standing on their own.

MediaTek points to Narad's deposition testimony, which states:

19 There is no doubt that the power management IC is also coupled  
 20 to power pins on the i.MX 31 in order to provide power in to the i.MX  
 21 31.

22 Dr. Vahid cited to an application note that described in detail  
 23 how an i.MX 31 and an associated PMIC would be connected pin by  
 24 pin.

25 From the perspective of the processor cores on the i.MX 31, the  
 26 power supply is the pin that is providing power in towards that core in  
 27 the same way that a sink in a house is a water supply.

28 Now, the power management IC is providing a variable voltage  
 through that pin in the same way that the reservoir -- kind of pipes in  
 the street are providing water to the water supply in your house.

So in my report, when I state that these are used with a power  
 management IC, what I'm explaining is that *the power management IC*

*provides that voltage, and the power supply within the chip provides that voltage to the elements within the chip.*

(Dkt. No. 303-29, Exh. 13 to Ewerdt, Narad Depo., at 454:10-455:14 [emphasis supplied].)

However, this new opinion does not create a triable issue. Narad's report fails to make any mention of the power pins theory, and Narad has not been given leave to supplement his report with these new opinions. The deposition testimony is inadmissible. *O2 Micro Int'l Ltd. v. Monolithic Power Sys., Inc.*, 467 F.3d 1355, 1368-69 (Fed. Cir. 2006) (new expert opinions properly excluded where proponent failed to disclose a report that "contain[s] a complete statement of all opinions to be expressed and the basis and reasons therefor" consistent with FRCP 26(a)(2)).

In short, MediaTek has not marshalled admissible evidence to show that the accused chips meet the "power supply" limitation. Thus, MediaTek has not created a triable issue on infringement of Claim 35 by the i.MX31, i.MX35, and i.MX50 chips, either based upon direct or indirect infringement. Having failed to do so, summary judgment of non-infringement as to the accused chips' infringement of Claim 35 is **GRANTED**.<sup>9</sup>

**B. Claim 11: Alleged Infringement of i.MX31, i.MX35, i.MX50, and i.MX6 Chips**

**1. "Plurality of Registers"**

With respect to Claim 11, Freescale argues that the i.MX31, i.MX35, i.MX50, and i.MX6 chips do not infringe on two grounds. One, they do not meet the "plurality of registers" limitation, or two, the "storing information indicating the clock frequency requirement" limitation.

Claim 11 describes a "processor comprising":  
one or more components receiving the at least one clock signal; and  
a controller ... adapted to determine a voltage requirement based on the clock  
frequency requirement of the processor ...;

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<sup>9</sup> The Court notes that it has stricken that portion of MediaTek's expert's report concerning the "power supply" limitation for the *iMX50 chip* as being inconsistent with MediaTek's infringement contentions. (See Order Granting In Part and Denying In Part Freescale's Motion to Strike Portions of Expert Reports, filed this date.) Thus, as to the iMX50 chips, MediaTek's evidence in opposition to summary judgment is not admissible. The Court further notes that MediaTek's infringement contentions do not mention the PMIC as a power supply for the i.MX50 chip. Freescale's motion for summary judgment of non-infringement *as to the i.MX50 chips only* is also **GRANTED** on that basis.

wherein the controller is coupled to at least one component by a *plurality of registers*, the plurality of registers *storing information indicating the clock frequency requirement* of the processor.

(’331 Patent, col. 15:43-58, emphasis supplied.)

The first dispute here centers on the scope of the phrase “plurality of registers.” Pursuant to the parties’ stipulated construction, Claim 11’s “plurality of registers” means: a “plurality of circuits capable of storing one or more bits.” (Dkt. No. 65, Supplemental Claim Construction Statement, at 1.)

Freescall argues that the component of the accused chips is, in fact, a “single register” holding a single piece of information, namely the frequency adjustment interrupt information (also called “FSVAI”). Freescall contends that a *single* register containing two bits used to represent direction cannot meet the plurality limitation. MediaTek responds that two circuits, each capable of storing one bit, would constitute a “plurality of registers,” consistent with the agreed construction.

MediaTek’s expert testified that the portion of the accused chips that he identifies as the “registers” are a specific type of circuit, called a “flip-flop” or “latch,” that stores just one bit of data. (Vahid Tr. 450:5-22 [agreeing that a latch or flip-flop is a circuit].) The accused chips contain two of these flip-flop circuits, one storing a “bit 0” and one storing a “bit 1.” (*Id.* at 449:21-450:22; *see also* Narad ’331 Infr. Rpt., Exh. C-1 at 34, Exh. C-2 at 25, Exh. C-3 at 35.) Thus, there is no dispute that there is more than one flip-flop circuit on the accused chips. Under the parties’ construction of “plurality of registers,” this evidence is sufficient to create, at least, a triable issue as to whether the accused chips practice the “plurality of registers” limitation of Claim 11. Consequently, summary judgment on these grounds is **DENIED**.<sup>10</sup>

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<sup>10</sup> Freescall’s argument that its registers are not identical to the ones shown in Figure 7 of the ’331 Patent is inapposite. (Freescall Mot. at 16.). The meaning of the term is not limited to single embodiment in the patent. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (“Although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.”)

1           **2. “Clock Frequency Requirement”**

2           Freescale’s second argument for non-infringement of Claim 11 of the ‘331 Patent is that the  
3 accused chips do not meet the “clock frequency requirement” limitation. The ‘331 Patent defines the  
4 term “clock frequency requirement” in the specification as follows:

5           The term “clock frequency requirement” refers generally to the clock frequency  
6 or set of clock frequencies provided to a processor that are necessary to support  
7 the tasks, functions, and/or computational requirements of a processor.  
(’331 Patent, 3:21-24.)

8           Freescale argues that the single piece of information, the frequency adjustment interrupt  
9 information, stored in the two flip-flop circuits described above does not constitute “information  
10 indicating a clock frequency requirement.” The frequency adjustment interrupt information in the  
11 flip-flop circuits does not express a “frequency” but just indicates whether a frequency change  
12 should occur and, if so, the direction in which frequency should be changed.

13           MediaTek counters that the two bits in the two flip-flop circuits indicate whether to increase  
14 clock frequency, decrease clock frequency, or leave the clock frequency unchanged, and that this  
15 information is sufficient to meet the “clock frequency requirement” limitation. MediaTek’s expert  
16 explained in his report that these bits are information about the clock frequency. (Narad Dec., Dkt.  
17 325-19, Exh. 1, Narad Opening Report, Exh. C-1 at 34, Exh. C-2 at 25-27, Exh. C-3 at 34-35.)

18           The ’331 Patent’s specification discloses that “registers” store “information indicating the  
19 frequency requirement of the processor” (*see* ’331 Patent col., 13:20-22) and “[e]ach register may  
20 store a binary indication as to whether the associated subsystem requires a particular clock signal, or  
21 the clock signal of a particular clock domain” (*id.* 13:24-27). The specification goes on to describe  
22 an example of the registers in an illustrative embodiment of the patent, stating:

23           For example, assume that register 610a’ corresponds to the frequency requirement  
24 of the DSP subsystem. According to the computational demands of the  
25 subsystem, the DSP may indicate which clock signals it requires in order to meet  
26 the current processing demands. The DSP may, for instance, before transitioning  
27 to an idle state, indicate such **a clock frequency requirement by writing a zero**  
**into each bit of register 610a’**. Alternatively, if the DSP still requires a system  
28 clock signal, for instance, even when in an idle state, **the DSP may indicate a 1 in**  
**the bit corresponding to the system clock**. The other subsystems of the processor

would similarly indicate which clock signals are required in order to perform the functions and/or computational tasks of a particular operating mode. As such, comparator 620' may *map the binary clock indications* to a location in memory storing a voltage level to support the clock signal configuration indicated by the frequency requirement stored in registers 610'.

(‘331 Patent, col. 13:31-48, emphasis supplied.) The Court concludes, based upon the information before it, that the clock frequency requirement described in the patent’s specification includes a clock frequency requirement that is simply a binary bit of information.

Accordingly, the proffered evidence is sufficient to create a triable issue of fact as to the accused chips’ infringement of Claim 11 of the ‘331 Patent. Summary judgment on these grounds is **DENIED**.

#### IV. CONCLUSION

As to non-infringement of Claims 1, 2, and 5 of the ‘845 Patent, summary judgment is **DENIED** in light of contrary opinions about how the MX6FAST3 arbiter operates “among” the other components required by the claim limitation.

As to non-infringement of Claims 21, 22, and 25 of the ‘845 Patent regarding arbitration among subsystems requests at the same priority level, summary judgment is **DENIED** based on a disputed of material facts as to the accused chips operation with respect to arbitration of requests with dynamic priority levels and allocation of priorities in a 75/25 bandwidth allocation scheme.

As to non-infringement of Claim 35 of the ‘331 Patent, summary judgment of non-infringement is **GRANTED** on the grounds that there is no dispute of fact, based upon admissible evidence, as to whether the accused chip meets the “power supply” limitation of the claim. The Court finds that MediaTek’s “power pin” theory for meeting this limitation is not admissible. Summary judgment is granted on both MediaTek’s direct and indirect infringement claims with respect to Claim 35 of the ‘331 Patent on the i.MX31, i.MX35, and i.MX50 chips.

As to non-infringement of Claim 11 of the ‘331 Patent regarding the “plurality of registers” and “clock frequency” limitations, summary judgment is **DENIED** as there are triable issues of fact based upon the experts’ opinions and the parties’ stipulated construction.

1 This order terminates the remaining issues in the underlying motion at Docket No. 303.

2 **IT IS SO ORDERED.**

3 Dated: June 20, 2014

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5 YVONNE GONZALEZ ROGERS  
6 UNITED STATES DISTRICT COURT JUDGE  
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